

# PhD Qualifiers Examination

# Computer Architecture

Spring 2009

NOTE:

1. This is a **CLOSED** book, **CLOSED** notes exam.
2. Please show all your work clearly in legible handwriting.
3. State all your assumptions.
4. There are **EIGHT** questions in total. Answer **any SIX** questions only.

## 1. Tomasulo's algorithm

Consider the following MIPS code:

```
Label:  L.D.   F2, 10(R2)
        SUB.D F2, F2, F4
        MUL.D F6, F0, F4
        ADD.D F0, F2, F10
        SUBI  R2, R2, 100
        BEQZ R2, Label
```

Show the execution of single issue Tomasulo algorithm in the form of status tables for the above code sequence for two iterations of the above loop. Assume the following:

- There are two FP ADD/SUB units, 2 FP MULT units, 4 load buffers and 2 store buffers.
- FP ADD/SUB takes 4 cycles, multiplications take 10 cycles, divide takes 20 cycles, and loads take 1 cycle for execution.
- The issue and write result stages each take 1 clock cycle
- Function Units are not pipelined and there is no forwarding between functional units; results are communicated by the CDB
- SUBI, BEQZ are integer instructions that take 1 clock cycle to execute

Show the status table (similar to the one in the text book) with three stages: *Issue*, *Execute* and *Write Result*.

## 2. Pipelining

- a) Name two RISC and two CISC processors. What are the main characteristics of RISC processors?
- b) Define (i) superscalar and (ii) super-pipeline concepts. Derive the equation for ideal speedup for a superscalar super-pipelined processor compared to a sequential processor. Assume  $N$  instructions,  $k$ -stage scalar base pipeline, superscalar degree of  $m$ , and superpipeline degree of  $n$ .

### 3. Performance:

For the same program, two different compilers are used. The table below shows the execution time of the two different compiled programs.

	Compiler A		Compiler B	
	# instructions	Execution Time	# instructions	Execution Time
Program 1	1.00 E+09	1s	1.20 E+09	1.4s
Program 2	1.00 E+09	0.8s	1.20 E+09	0.7s

- Find the average CPI for each program given that the processor has a clock cycle time of 1ns.
- Assume the average CPIs found in part (a), but that the compiled programs run on two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code?
- A new compiler is developed that uses only 600 million instructions and has an average CPI of 1.1. What is the speed-up of using this new compiler versus using Compiler A or B on the original processor of part (a)?

**4. Briefly answer the following questions:**

- a) What is the difference between computer architecture and computer organization?
- b) What are the two locality principles observed with respect to user programs? How are these principles exploited in computer design?
- c) What is virtual memory? Explain the need for virtual memory.
- d) What are the main differences between a multi-processor system and a multi-computer system?
- e) In a shared memory system, explain two schemes to maintain cache-coherence.

### 5. Data Dependency and Hazards:

Consider the following MIPS assembly code:

```
LD    R1, 45(R2)
ADD   R7, R1, R5
SUB   R8, R1, R6
OR    R9, R5, R1
BNEZ  R7, target
ADD   R10, R8, R5
XOR   R2, R3, R4
```

- a) Identify each type of data dependency; list the two instructions involved; identify which instruction is dependent; and, if there is one, name the storage location involved.
- b) Use MIPS five-stage pipeline (fetch, decode, register, execute, write-back) and assume a register file that writes in the first half of the clock cycle and reads in the second half cycle. Which of the dependencies that you found in part (a) become hazards and which do not? Why?

### 6. Cache Mapping:

A computer system has a 128 byte cache. It uses four-way set-associative mapping with 8 bytes in each block. The physical address size is 32 bits, and the smallest addressable unit is 1 byte.

- a) Draw a diagram showing the organization of the cache and indicating how physical addresses are related to cache addresses.
- b) To what block frames of the cache can the address  $000010AF_{16}$  be assigned?
- c) If the addresses  $000010AF_{16}$  and  $FFFF7Axy_{16}$  can be simultaneously assigned to the same cache set, what values can the address digits  $x$  and  $y$  have?

## 7. Assembly Programming:

Consider a hypothetical machine called SIC, for Single Instruction Computer. As its name implies, SIC has only one instruction: subtract and branch if negative, or `sbn` for short. The `sbn` instruction has three operands, each consisting of the address of a word in memory:

```
sbn a, b, c, #Mem[a] = Mem[a] - Mem[b]; if (Mem[a] < 0) go to c
```

The instruction will subtract the number in memory location `b` from the number in location `a` and place the result back in `a`, overwriting the previous value. If the result is greater than or equal to 0, the computer will take its instruction just after the current instruction. If the result is less than 0, the next instruction is taken from memory location `c`. SIC has no registers and no instructions other than `sbn`.

(a) Identify what the following does:

```
start:      sbn  temp, temp, .+1
            sbn  temp, a, .+1
            sbn  b, b, .+1
            sbn  b, temp, .+1
```

In the above program `+.1` means “the address after this one.”

(b) Write a SIC program to add `a` and `b`, leaving the result in `a` and leaving `b` unmodified.



### **8. RISC CPU Design:**

Design a (very) simple CPU for an instruction set that contains only the following four instructions: lw (load word), sw (store word), add, and jump (unconditional branch). Assume that the instruction formats are similar to the MIPS architecture. If you assume a different format, state the instruction formats. Show all the components, all the links, and all the control signals in the datapath. You must show only the minimal hardware required to implement these four instructions. For each instruction show the steps involved and the values of the control signals for a single cycle implementation.